THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JANUSZ K. BALICKI, BEZHAD NOUBAN
and KHUSROW KIANI

Appeal No. 96-1286
Application 08/259,360[1]

ON BRIEF

Before URYNOWICZ, THOMAS and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-13. No claim has been allowed.

References relied on by the Examiner

Fuss	3,702,393	Nov. 7, 1972

[1] Application for patent filed June 14, 1994.

Nissen et al. (Nissen) 4,152,778 May 1, 1979

"Appellant’s admitted prior art on pages 1-2 and Fig. 1 of the specification" (see examiner’s answer at page 2)

The Rejections on Appeal

Claims 1-13 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over "appellant's admitted prior art on pages 1-2 and Fig. 1 of the specification in view of Nissen et al. or Fuss."

The Invention

The invention is directed to a method and apparatus for a look-up table built on programmable architecture memory elements. According to the appellants, the number of programmable architecture elements required for a lookup-table performing a number of specific multi-variable logic functions is reduced, as compared to prior art lookup-table methods and devices. Claims 1 and 9 are representative and are reproduced below:

1. A method for designing a limited function look-up table having a reduced number of programmable architecture elements, the look-up table having a plurality of inputs, the method comprising:

choosing a plurality of logic functions to be performed by the look-up table;

determining an output state for each set of input variables, each output state comprising an array of responses of the plurality of logic functions to a particular set of input variables;

forming groups of the output states, the groups of output

states comprising identical output states;

eliminating selected groups of the output states, the selected groups not requiring programmable architecture elements; and

assigning a programmable architecture element for each remaining group of output states, each programmable architecture element being for storing the responses of a particular output state.

9. A look-up table architecture for performing AND, OR, and XOR logic functions, the look-up table architecture comprising:

a look-up table output terminal;

no more than four programmable architecture elements, the programmable architecture elements for storing outputs, the outputs being organized into output states, each output state comprising responses of the AND, OR, and XOR logic functions to a particular set of input variables, each programmable architecture element being for storing the outputs of a particular output state;

a plurality of logic gates coupled to the programmable architecture elements and the look-up table output terminal, the logic gates for gating the outputs stored in the programmable architecture elements to the look-up table output terminal; and

at least three input terminals connected to the logic gates, signals being supplied to the input terminals, the signals defining an input state to control the plurality of logic gates, thereby facilitating the gating of an output stored in a particular programmable architecture element to the output terminal.

Opinion

We reverse.

A reversal is not an affirmative indication that the claims on appeal are patentable over prior art, even those cited and applied by the examiner. We focus only on the examiner's rationale and stated position for rejecting these claims.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one with ordinary skill in the art would have been led to modify or combine prior art references to arrive at the claimed invention. Such reasons must stem from some teaching, suggestion, or implication in the prior art as a whole or knowledge generally possessed by one with ordinary skill in the art. Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985),

cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. See, e.g., In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

We find that the examiner failed to set forth sufficient factual basis concerning prior art teachings and suggestions therefrom to account for all the differences between the claimed invention and the prior art. Specifically, on page 2 of the final Office action (Paper No. 12), the examiner recognized and acknowledged that the appellants' own admitted prior art does not disclose following the steps of appellants' claim 1:

1. forming groups of the output states;
2. eliminating selected groups of output states; and
3. assigning a programmable architecture element for each remaining group of output states.

According to the examiner, this deficiency is made up by either Nissen or Fuss, in the alternative. In that regard, the final Office action states (page 2, line 16 to page 3,

line 1):

> Nissen et al. disclosed the steps of forming groups of the output states, eliminating selected groups, and assigning a programmable architecture element for each remaining group (col. 4, line 41, et seq.). Fuss also disclosed the steps of forming groups of the output states, eliminating selected groups, and assigning a programmable architecture element for each remaining group (col. 2, line 29, et seq.).

Just specifically how each of Nissen and Fuss discloses (1) forming groups of output states where each output state comprises an array of logical function responses to a plurality of inputs, (2) eliminating selected groups of the output states which do not require programmable architecture elements, and (3) assigning a programmable architecture element for each of the remaining groups of output states, has not been adequately explained. Neither the appellants nor this Board should have to guess or speculate on what factual findings on the scope and content of the prior art the examiner has in mind.

In the disclosure of each of Nissen and Fuss, it is uncertain what the examiner regards as the logical functions, the logical function responses, the plurality of input variables, an output state representing an array of logical function responses to the plurality of inputs and groups of

output states. The appellants dispute that either Nissen or Fuss discloses these features of the claimed invention. Without clear findings for these claim elements, it cannot be said that a sufficient factual basis has been established in support of a rejection for obviousness. Insofar as these claim features are concerned, the cited portions of Nissen and Fuss do not speak for themselves in the absence of a reasonable explanation by the examiner.

In response to the appellants' assertion that neither Nissen nor Fuss discloses the above-quoted features of the claimed invention, the examiner again fails to make specific factual findings with regard to the features at issue or explain how they are found in the disclosure of Nissen or Fuss. Instead, the examiner responds (examiner's answer at 5) by stating merely that "both Nissen et al. and Fuss teach the well known capability of reducing the number of memory elements by grouping identical (or redundant) data." The problem with that approach, however, is that the claims do not just broadly recite reducing the number of memory elements by grouping identical data. Rather, the claims include numerous specific claim elements or specific steps performed on these

claim elements, all of which must be accounted for in establishing a case of prima facie obviousness.

Moreover, neither Nissen nor Fuss is directed to a look-up table implementing logical functions for multiple variables. The general idea of grouping identical data to reduce memory requirements would not have reasonably suggested the specific features of the appellants' claims concerning logical functions, grouping of output states each representing an array of logical function responses, elimination of selected output states and assignment of a programmable architecture element to the remaining output states. The mere fact that the prior art may be modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor. Para-Ordnance Mfg. Inc. v. SGS Importers Int'l Inc., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), cert. denied, 117

S. Ct. 80 (1996). The appellant is correct that merely citing a reference which describes a similar generic goal is not sufficient to obviate the specific limitations of the appellants' claimed invention.

Independent claims 5, 9, and 13 are apparatus claims and do not recite the method steps discussed above in connection with the deficiencies in the examiner's findings. However, they each recite a specific look-up table architecture implementing a plurality of logical functions. And like claim 1, they each require the implementation of multi-variable logical functions, output states each representing the logical function responses for a particular set of input variables and programmable architecture elements each for storing the responses of a particular output state. More importantly, they each recite a limit on the number of programmable architecture which is less than that necessary for implementing a look-up table capable of performing all possible logic functions of the plurality of input variables. In that regard, claims 9 and 13 require at least three input terminals but no more than four programmable architecture elements (claim 9) or programmable static random-access-memory

cells (claim 13). Implicit in this look-up table architecture is that those output states not requiring a programmable architecture element or those non-occurring output states are eliminated or ignored. The output states are those of multi-variable logical functions.

Accordingly, the above discussion concerning inadequate findings by the examiner as to claim 1 are also applicable to claims 5, 9 and 13. In any event, the examiner's broad and general discussion of Nissen and Fuss does not constitute a sufficient factual basis to modify the appellants' admitted prior art to arrive at a look-up table for implementing a limited number of logic functions with fewer programmable architecture elements than that necessary for performing all possible logic functions of the input variables. The mere fact that the prior art may be modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Obviousness may not be established using hindsight or in view

of the teachings or suggestions of the inventor. Para-Ordnance Mfg. Inc. v. SGS Importers Int'l Inc., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), cert. denied, 117 S. Ct. 80 (1996).

The initial burden is on the examiner to establish a prima facie basis to reject the claims. In re Oetiker, 977 F.2d 1443,
1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The examiner must provide an adequate factual basis to support an obviousness conclusion. In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 178 (CCPA 1967). Here, the examiner's findings are too vague and incomplete for supporting a case of prima facie obviousness. The necessary burden has not been met.

For the foregoing reasons, we do not sustain the rejection of claims 1-13 under 35 U.S.C. § 103 as being unpatentable over the appellants' own admitted prior art, in view of either Nissen or Fuss.

Conclusion

The rejection of claims 1-13 under 35 U.S.C. § 103 as being unpatentable over the appellant's admitted prior art and

either Nissen or Fuss is reversed.

REVERSED

STANLEY M. URYNOWICZ Administrative Patent Judge	)
JAMES T. THOMAS Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
JAMESON LEE Administrative Patent Judge	)

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